Ultrathin Gate Dielectric Enabled by Nanofog Aluminum Oxide on Monolayer MoS_2

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***Abstract*— Field-effect transistors (FETs) based on two-dimensional (2D) semiconductors must have ultrathin gate dielectrics in order to achieve low voltage operation. Here we achieve conformal HfO_2 gate dielectrics on monolayer MoS_2 with the aid of an AlO_x seed layer deposited by "nanofog," a low temperature process at 50 °C. We study the uniformity of the nanofog layer as a function of its deposition temperature, and we also compare FETs fabricated with nanofog AlO_x seed vs. electron-beam evaporated Al seed layers, followed by HfO_2 dielectric. With the nanofog seed, we achieve subthreshold slope < 100 mV/dec at room temperature and equivalent oxide thickness (EOT) of 1.3 nm. Devices with nanofog exhibit nearly hysteresis-free behavior, unlike those with the Al seed, consistent with the subthreshold data showing fewer interface defects with nanofog seed layers. The "nanofog" process is thus established as a low-temperature, industry-compatible seed layer for high-κ dielectric deposition onto 2D semiconductors.**

Keywords*— *Nanofog, AlO_x, 2D, MoS_2, EOT

I. Introduction

Two-dimensional (2D) monolayer semiconductors are promising materials for electronics owing to their ultrathin (sub-1 nm) nature. In particular, 2D transition metal dichalcogenides (TMDs) have gained attention as semiconductors with larger electronic band gaps than Si, maintaining good carrier mobility at monolayer (1L) thickness [1,2]. Relatively low TMD growth temperatures (< 600 °C) have also been achieved, compatible for integration with existing Si technology [3].

Due to inert surfaces without dangling bonds of 2D TMD channel materials, it is challenging to perform uniform atomic layer deposition (ALD) of ultrathin dielectrics onto them. Studies have shown that adding a thin evaporated seed layer on 2D TMDs provides nucleation for ALD of a high-κ dielectric. For example, metals such as Al were e-beam evaporated on 1L MoS_2 to form a thin seeding layer to enable ALD without damage [4]. However, such seed layer processes are directional and cannot be deposited conformally, e.g., on gate-all-around FETs or high-aspect ratio features.

Previous efforts have shown that AlO_x deposited by a unique process called "nanofog" provides an excellent interfacial layer for gate dielectrics on nanomaterials with inert surfaces, such as carbon nanotubes [5, 6]. Nanofog is a low-temperature deposition process that involves ALD with a chemical vapor deposition (CVD) component, and it has been reported that nanofog AlO_x forms a low interface trap density with exfoliated MoS_2 as determined from metal-oxide-semiconductor capacitor structures [7].

In this work, nanofog is shown to provide a low defect seed layer for fabricating top-gated (TG) FETs using CVD-grown 1L MoS_2 as the channel material. First, uniformity of the nanofog film on CVD 1L MoS_2 as a function of deposition temperature is determined using Auger electron spectroscopy (AES). Second, the generation of defects by a seed layer of nanofog AlO_x and e-beam evaporated Al seeding layer on MoS_2 are investigated using Raman spectroscopy. Third, using the optimal deposition conditions of nanofog on MoS_2, top-gated 1L MoS_2 FETs are fabricated using a bilayer gate dielectric of nanofog AlO_x followed by ALD HfO_2 to achieve ultrathin EOT devices while maintaining low gate leakage current.

II. Sample Preparation

Fig. 1(a) shows the cross-section schematic of the TG MoS_2 FET devices, and the fabrication process steps are as follows. First, 1L MoS_2 is grown by solid-source CVD at 700 °C on thermally oxidized SiO_2 of thickness 85 nm on p^{++} Si substrates, which also serve as global back-gates [8]. The channel region is patterned by XeF_2 dry etching. Next, source/drain contacts are patterned and deposited with e-beam evaporated Au, without an adhesion layer to obtain lower contact resistance [1]. For the top-gate dielectric, nanofog AlO_x is deposited at 50 °C as the seeding layer, followed by thermal ALD of HfO_2 at 200 °C using tetrakis(dimethylamido)hafnium and H_2O as the precursors. Finally, the Pd top-gate metal is deposited by e-beam evaporation and subsequent lift-off.

To minimize the resistance from the ungated channel area, the top gate overlaps with the source and drain. For this study, channel lengths ranging from 200 nm up to 3 μm with channel widths of 2 μm are fabricated. The electrical measurements are performed at room temperature in vacuum (~10^{-5} Torr) after annealing at 150 °C in vacuum for 2 hours to remove water absorbents.

Fig. 1(b) shows a schematic of the samples prepared for the Raman studies, atomic force microscopy (AFM) and AES, with similar 1L MoS_2 grown on SiO_2/Si as for the FETs. Then, the seeding layer of either nanofog AlO_x or evaporated Al are deposited. To obtain a consistent thickness, 2 nm of nanofog AlO_x is deposited whereas 1 nm of Al is evaporated, which increases

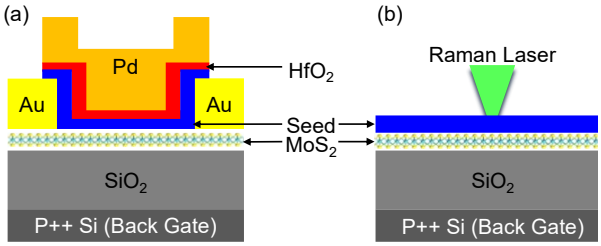

Fig. 1. (a) Top-gated MoS_2 transistor cross-section schematic in the active device region. Layer in blue is the nano-fog seeding layer and layer in red is the ALD HfO_2. (b) Sample preparation for Raman spectroscopy, AFM and AES. Layer in blue is the seeding layer which is deposited on a monolayer MoS_2.

to ~2 nm AlO_x due to the volume expansion after oxidation. For Raman spectroscopy, we use a laser source with 532 nm wavelength and 2.5% incident power, which corresponds to 0.12 mW.

III. Results and Discussion

A. AES, AFM and Raman Spectra

We first investigate the optimal deposition conditions of the nanofog seed layer onto 1L MoS_2. Nanofog AlO_x is deposited at temperatures ranging from 50 °C to 70 °C and thicknesses from 1 nm to 5 nm. Temperatures higher than this range do not provide a uniform AlO_x layer for 1L MoS_2, confirmed by AFM. AES is performed on the samples to check for pinholes on the nanofog film; note this is not spatially resolved so the technique detects pinholes when they are a large fraction of the surface area. Table 1 shows the elemental information of the surface. At the higher deposition temperature of 70 °C, there are at least 5% signals of the Mo and S from the surface even when using 5 nm of nanofog AlO_x. This indicates possible pinholes in the nanofog AlO_x, through which the signals from the 1L MoS_2 underneath the AlO_x layer are detected. Mo and S signals are reduced to 3% on samples with 5 nm of nanofog deposited at 50 °C; this corresponds to the noise level of the instrument and thus can be neglected. A similar trend is found with 1 nm-thick nanofog. As the deposition temperature is reduced from 70 °C to 50 °C, the signals from Mo and S are significantly reduced, indicating less pinhole formation in the nanofog AlO_x film deposited at a lower temperature.

Fig. 2(a) shows the AFM image of the sample with nanofog deposited at 50 °C and this confirms the absence of pinholes on the surface. This validates that nanofog deposited at 50 °C provides a uniform AlO_x layer, and this deposition condition is subsequently used for all the sample preparation and fabrication of top-gated MoS_2 FETs with nanofog AlO_x seeding layer.

TABLE I.

Deposition Temperature	Nanofog Thickness	S (%)	Mo (%)	Al, O, Si (%)
50 °C	1 nm	3.0	4.9	92.1
60 °C	1 nm	12.1	7.2	80.7
70 °C	1 nm	38.2	11.2	50.6
50 °C	5 nm	1.6	2.5	95.9
70 °C	5 nm	6.4	5.1	88.5

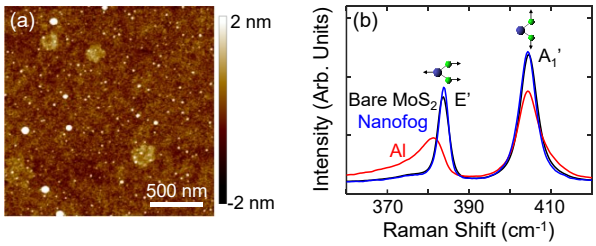

Fig. 2. (a) Atomic force microscopy (AFM) image of nanofog AlO_x ~2 nm on 1L MoS_2. The surface root-mean-square roughness is 3 Å, which is comparable to bare CVD 1L MoS_2. (b) Raman spectra of bare 1L MoS_2 (black), nanofog AlO_x on 1L MoS_2 (blue), and evaporated Al on 1L MoS_2 (red).

Fig. 2(b) shows the Raman spectra comparing nanofog AlO_x and evaporated Al. Previous studies have shown that evaporated Al on 1L MoS_2 does not damage the material and provides *n*-type doping [9]. However, in the case of nanofog AlO_x, the E' and A_1' Raman peaks of 1L MoS_2 are preserved without any broadening, indicating the nanofog AlO_x does not react with or damage 1L MoS_2, and does not provide doping or strain to the material, unlike the evaporated Al seeding layer.

B. Comparison of Top-Gated MoS_2 FETs

To compare the electrical performance of the nanofog and evaporated Al seeding layers, top-gated (TG) 1L MoS_2 FETs are fabricated using bilayer of HfO_2 and AlO_x seeding layer as the top gate dielectric. For the seeding layers, either ~3 nm of nanofog AlO_x is deposited or ~1.5 nm of Al (which becomes ~3 nm of AlO_x) is evaporated on 1L MoS_2, followed by 10 nm of ALD HfO_2. Fig. 3 shows the measured TG transfer characteristics of two typical devices with 3 µm long channel. In the case of the evaporated Al seeding layer, a wider hysteresis window is observed compared to nanofog. The hysteresis in MoS_2 FETs originates from the position of the defect band in the gate dielectric relative to the conduction band of 1L MoS_2. When the defect band of the gate dielectric layer is within the band gap of the channel material, threshold voltage changes depending on the gate voltage sweeping direction due to the number of the charged interfacial traps [10]. The smaller hysteresis in the nanofog seeding layer implies that nanofog AlO_x provides a higher quality aluminum oxide on the MoS_2, with lower interface trap density.

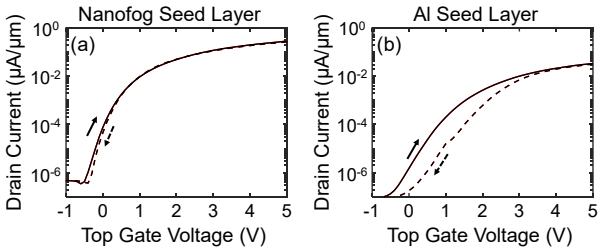

Fig. 3. Drain current (I_D) vs. top gate voltage (V_{TG}) curves for (a) nanofog AlO_x and (b) evaporated Al seeding layer. The back gate is at 0 V, and source-to-drain voltage bias V_{DS} = 0.1 V is applied. Devices are 3 µm long and 2 µm wide. Solid and dashed lines represent forward and reverse sweeps of the V_{TG}, respectively.

Key differences can also be seen in the subthreshold slopes of the two device types. As the thicknesses and the materials for the top dielectric stack are the same, the top gate oxide capacitances of nanofog and evaporated Al are assumed to be the same. From the two seeding layers, the subthreshold slope when using nanofog seeding layer is steeper compared to the case of evaporated Al seeding layer at any fixed subthreshold current. This suggests that the interface trap capacitance in nanofog is smaller, and hence the nanofog AlO_x provides a seeding layer with lower interface trap density than evaporated Al [10].

C. TG MoS_2 FET with Scaled Dielectric Stack

Next, we reduce the gate dielectric stack to achieve thinner EOT. Top-gated MoS_2 FETs are fabricated using bilayer dielectric of ~2 nm nanofog AlO_x followed by just ~2 nm or ~3 nm of ALD HfO_2.

Fig. 4(a) shows the cross-section TEM image of a 200 nm channel length device. The TEM shows the top gate is overlapped with the source/drain structure to mitigate the ungated channel resistance. Fig. 4(b) shows the zoomed-in image of the gate stack; the 1L MoS_2 does not show any discontinuity or physical damage from processing. The TEM shows differences in the ALD HfO_2 thickness when it is deposited on samples with nanofog on MoS_2 compared to on bare Si. The ALD HfO_2 thickness is ~3 nm on the nanofog seeding layer on MoS_2 whereas on bare Si with the same number of cycles, it is ~5 nm. It is hypothesized that due to the small gaps in the ultrathin nanofog film, the first few cycles of ALD HfO_2 are consumed to fill in those pinholes. A similar trend is observed with the thinner HfO_2 sample where the thickness of HfO_2 on nanofog AlO_x from the TEM is ~2 nm but the thickness on bare Si is ~3 nm, implying that the first cycles of ALD are consumed for filling in the gaps. Fig 4(c) shows the STEM EDS, displaying the elemental distribution of the gate stack. The gate stack in this work is Pd, HfO_2, AlO_x, MoS_2 and SiO_2 from top to bottom. Fig. 4(d) shows the line profile from the EDS image in Fig. 4(c) that further confirms that the AlO_x is between MoS_2 and HfO_2. Fig. 4(e) and 4(f) show that the device that was used for this TEM cross-section works well with an on-off ratio of more than 10^6 and the drain current reaching more than 100 µA/µm at V_{DS} = V_{TG} = 1 V and V_{BG} = 50 V with little hysteresis. From the physical thicknesses of ALD HfO_2 ~2 nm with a κ ~22 on nanofog AlO_x ~2 nm with a κ ~8 from the thinner stack, the EOT of the gate stack is calculated to be 1.33 nm.

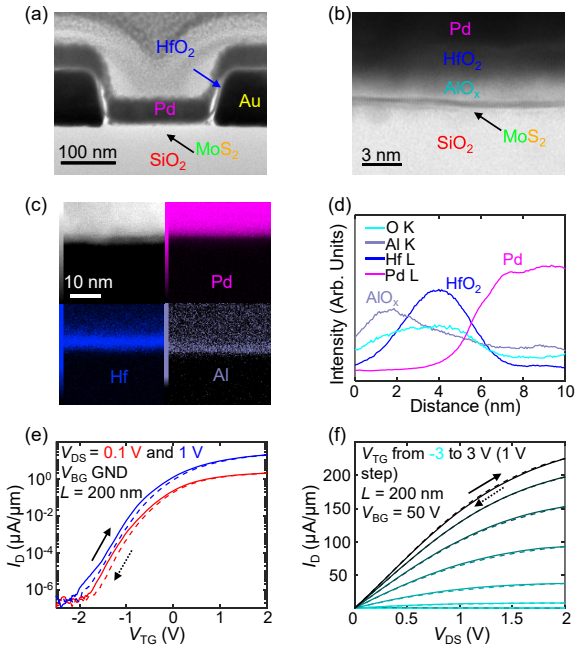

Fig. 4. (a) Cross-section transmission electron microscope (TEM) image of the active region of a transistor with ~200 nm channel length from the thicker stack. (b) Zoomed-in scanning TEM (STEM) image in bright-field mode showing the gate stack on 1L MoS_2. (c) STEM high-angle annular dark-field image (HAADF) (top left) and its energy dispersive spectroscopy (EDS) showing the elemental distribution of the gate stack of Pd (top right), Hf (bottom left), and Al (bottom right), and (d) line profile from center of MoS_2 (at 0 nm) to the top gate (at 10 nm). Electrical characterization of the 200 nm length device showing (e) I_D-V_{TG} at V_{BG} = 0 V and (f) I_D-V_{DS} at V_{BG} = 50 V. Arrows mark solid and dashed lines

Fig. 5 shows the device transfer characteristics from bilayer dielectric of ~2 nm nanofog AlO_x followed by ~2 nm of ALD HfO_2. Fig. 5(a) shows that the 3 µm long channel device has an on-off ratio of more than 10^6, which is limited by the instrument noise floor. In all the long channel cases, almost no hysteresis is observed and considering that the hysteresis is a function of the applied gate voltage range, this shows that nanofog AlO_x provides low interfacial defect concentration to 1L MoS_2. Fig. 5(b) shows the I_D-V_D curve of the same device with a positive threshold voltage. Fig 5(c) shows that the subthreshold slope (SS) of the device reaches sub-100 mV/dec and may be expected to be lower as the measurement is limited by the instrument noise floor. The gate leakage current of the device is less than $5x10^{-8}$ A/cm^2 at V_{DS} = V_{GS} = 1 V at V_{BG} = 0 V, which is limited by the instrument, and this is expected to be lower with reduced overlap of top gate to source/drain. Fig. 5(d) shows the I_D-V_{TG} curve at various V_{BG} biases. The threshold voltage from the top gate sweep at different back gate biases are plotted as a function of the V_{BG}. The magnitude of the slope from the linear region in the inset of Fig 5(d) represents the ratio of the oxide capacitances of the back gate and the top gate [11]. Since the thermally oxidized SiO_2 (~85 nm) is used for the back gate dielectric, we can calculate the back gate oxide capacitance and

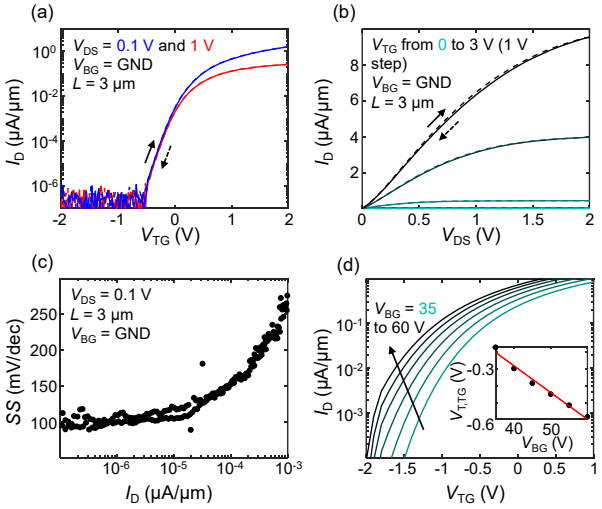

Fig. 5. (a) I_D-V_{TG} and (b) I_D-V_D curves of the same device. (c) Subthreshold slope as a function of drain current. (d) I_D-V_{TG} at V_{DS} = 0.1 V measured at various V_{BG} biases with 5 V step and the threshold voltage from the top gate sweep as a function of V_{BG} in the inset figure.

extract the top gate oxide capacitance from that slope.

The extracted EOT from this calculation is 1.35 nm, which matches the EOT from the physical thicknesses based on the cross-section TEM image. Further EOT scaling can be achieved by scaling the nanofog seeding layer from 2 nm and using 1 nm nanofog seeding layer followed by 3 nm HfO_2 should enable sub-1 nm EOT.

Fig. 6(a) shows the TG transfer curves of multiple devices with various channel lengths using 2 nm nanofog AlO_x and 2 nm ALD HfO_2. Using the constant current method to extract the threshold voltage from the top gate sweep, a positive threshold voltage in the long channel devices (L=1 µm and 3 µm) is observed. As the channel length is scaled from 1 µm down to 200 nm, the subthreshold slope increases. This is due to the thick back gate oxide of ~85 nm SiO_2 while using ultrathin top gate oxide with total physical thickness of ~5 nm. Previous studies have shown that due to the large discrepancy of the physical dielectric thicknesses at the top and bottom, scaling the channel length aggravates the subthreshold slope when the channel thickness is ultrathin, and this is expected to be mitigated with scaling of the back gate dielectric [12]. As shown in Fig. 6(b), with scaling of the channel length, the threshold voltage from the top gate sweep rolls off, which is a sign of short-channel effects. These effects are expected to be alleviated by using a thinner back gate dielectric or a high- κ/metal gate substrate.

IV. Conclusion

TG MoS_2 FETs using nanofog AlO_x seeding layer provide an excellent interface with nearly hysteresis-free behavior with DC sweep and sub-100 mV/dec subthreshold slope. An EOT of ~1.3 nm is achieved using a bilayer top gate dielectric of nanofog ~2 nm and ALD HfO_2 ~2 nm. At this EOT, the gate leakage current is less than 5×10^{-8} A/cm^2 at $V_{DS} = V_{GS} = 1$ V and $V_{BG} = 0$ V proving a suitable gate dielectric for fabricating TG 1L MoS_2 FETs. EOT is expected to be improved by aggressive scaling of the nanofog seeding layer thickness, since in this work, the AlO_x thickness used is relatively thick (~2 nm). As the nanofog is a conformal deposition process, these results envision the potential of achieving gate-all-around devices using 2D channels with the gate dielectric of sub-1 nm EOT.

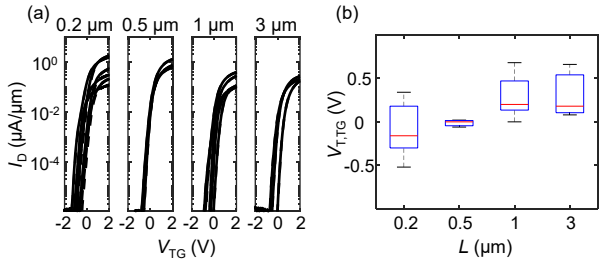

Fig. 6. (a) Top gate transfer characteristics (I_D-V_{TG}) at $V_{BG} = 0$ V and $V_{DS} = 0.1$ V. Solid line and dashed line represent forward sweep and reverse sweep, respectively, which show nearly negligible hysteresis. (b) Box plot showing the top gate threshold voltage of multiple devices on the same chip with different channel lengths. For each length of 200 nm, 500 nm, 1 µm and 3 µm, the number of devices measured are 6, 3, 5 and 3 respectively. Threshold voltage in this case was extracted by constant current method by setting the off-current at 10^{-2} µA/µm.

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